UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,894	08/11/2004	Kuen-Suey Hou	MTKP0123USA	4893

27765 7590 08/25/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,894	HOU ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12 and 13* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/9/2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No.6,147,530, issued to Nogawa.

As per claim 1, Nogawa discloses a phase locked loop PLL (figure 2) generating a phase locked signal (the OF signal) and adjusting a frequency of the phase locked

signal according to an incoming signal (this is the function of any PLL, the incoming signal is the ID signal), the PLL comprising:

an oscillator (VCO 5) for generating the phased locked signal (the OF signal); and

a frequency detection module (frequency comparator 2) electrically coupled to the oscillator (the frequency comparator 2 is coupled to the VCO 5 through the divider 6) for detecting two regular patterns in the incoming signal (figure 6 is the detailed of the frequency comparator, figure 7 explains the operation, the two regular patterns are sync patterns of the EFM modulation signal, column 12, lines 48-65 and the clock signal (since the clock signal is based on the incoming signal)), calculating a number of periods of the phase locked signal corresponding to a distance between the two regular patterns (column 14, lines 31-41), and controlling the oscillator to adjust the frequency of the phase locked loop signal according to the number of periods (the frequency comparator 2 outputs FCUP and FCDN signals to control the VCO 5, column 15, lines 1-29).

As per claim 2, Nogawa further discloses the frequency detection module comprises:

a pattern detector (frame generating counter 25) for detecting the two regular patterns (the sync patterns of the EFM modulation signal, column 12, lines 48- and the clock signal (since the clock signal is based on the incoming signal)see column 18 lines 60 -63) in the incoming signal;

a counter (counter 212 and peak and bottom hold units 22 and 23) electrically coupled to the pattern detector for calculating the number of periods of the phase locked signal corresponding to the distance between the two regular patterns; and

a comparator (frequency error output unit 24) electrically coupled to the counter for comparing the number of periods with a predetermined value (SYNC pattern SY, column 15, lines 11 and 27) to generate A control signal (FCUP and FCDD, and using the control signal to control the oscillator to adjust the frequency of the phase locked signal.

As per claim 3, the recited limitation is described in column 15, lines 1-29.

As per claim 4, the recited control interface reads on the charge pump circuit 8 shown in figure 2 which provides the signal FVP for controlling the frequency of the OF signal.

As per claim 5, the recited limitations are described in column 12, line 48, and lines 60-64.

As per amended claim 6, Nogawa's discloses the invention with a current controlled oscillator. (See column 16 lines 21-27).

As per claim 7, this claim is merely method to operate the PLL having the structure noted in claim 1. Since Nogawa teaches the circuit, the method to operate is inherently disclosed.

As per claims 8-10, these claims are rejected for the same reasons noted in claims 2-3 and 5, respectively.

With respect to claims 12-13, the sampling interval would determines if frames the periods are calculated based on adjacent or non-adjacent frames. Since the sampling interval can be adjusted these claims are inherent in the operation of the circuit.

Allowable Subject Matter

4. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With regard to claim 11, the prior art of record fails to suggest or disclose a Phase Locked Loop comprising a frequency detector in combination with a multiplexor with the functionality as recited in the claim.

Response to Arguments

5. Applicant's arguments filed 6/9/2006 have been fully considered but they are not persuasive.

With regard to the applicant's argument that "Ngoawa does not teach calculating a number of periods of the phase locked signal corresponding to a distance between the two regular patterns", the examiner disagrees. According to applicant "the pulse width counting unit 21 of frequency comparator 2 merely calculates a period between subsequent edges". Using applicants own statement a calculated period between subsequent edges still reads on the applicants claim because a period is still a number of periods (that number being 1) and a distance between the two regular patterns is inherent with the recitation of "between subsequent edges". Since each frame must incorporate the SYNC signal the regular pattern SYNC signals are also in two different frames as indicated in claim 1.

With regard to the applicant's argument "Nogawa does not teach adjusting the frequency of the phase locked loop signal according to the number of periods between two regular patterns", the examiner disagrees. Because a SYNC signal is in each of the EFM frames and a clock signal is also in each of the frames the examiner maintains the SYNC signal is a regular SYNC pattern and the clock signal is a regular pattern.

With regard to the applicants argument Nogawa "does not teach a counter for calculating the number of periods of the phase locked signal corresponding to the distance between two regular patterns ", the examiner disagrees. The counter counts up at every period of inverse regenerated clock and resets in reference to the sync pattern.

With regard to the applicants argument "Nogawa fails to teach or suggest using a numerical controlled oscillator or a current controlled oscillator in PLL to generate an

oscillation signal" the examiner disagrees. In column 16 lines 21-27 Nogawa teaches "it is needless to say that instead of VCO, a current controlled oscillator (ICO) may be used without deviating from the spirit of the present invention.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KEA
8/16/2006

Quan Tra
Primary Examiner